IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): M. Kapur et al.
Docket No.: YOR920030306US1
Serial No.: 10/650,222
Filing Date: August 28, 2003
Group: 2138
Examiner: Saqib Javaid Siddiqui

Title: Self-Synchronizing Pseudorandom Bit Sequence Checker

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter referred to as "Appellants") hereby appeal the final rejection of claims 1-17 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corporation, as evidenced by an assignment recorded August 28, 2003 in the U.S. Patent and Trademark Office at Reel 14479, Frame 375. The assignee, International Business Machines Corporation, is the real party in interest.

RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals or interferences.

STATUS OF CLAIMS

Claims 1, 4-6, 9-12 and 17 stand finally rejected under 35 U.S.C. §102(b). Claims 2, 3, 7, 8 and 13-16 stand finally rejected under 35 U.S.C. §103(a). Claims 1-17 are appealed.

STATUS OF AMENDMENTS

There was a minor amendment filed subsequent to the final rejection, which addressed an alleged antecedent basis issue in dependent claim 9. In an Advisory Action dated October 27, 2006, the Examiner indicated that the amendment was entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a method of checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device. The method comprises the steps of delaying the PRBS received by the device to generate a delayed PRBS, detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device, and prohibiting propagation of the detected error bit in the delayed PRBS, wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

As explained at page 2, lines 1-7, of the present specification, the methodology advantageously provides that, for a given clock cycle, the presence of an error bit in the PRBS generated by the device is detected. The error bit represents a mismatch between the PRBS input to the device and the PRBS output from the device. Then, propagation of the error bit is prohibited for subsequent clock cycles. The prohibition step/operation may serve to avoid multiple errors being counted for a single error occurrence and/or masking errors in the PRBS output by the device.

The present specification provides an illustrative embodiment of the elements of claim 1 at page 6, line 10, through page 8, line 7, in the context of FIGs. 4 and 5.

More particularly, FIG. 4 illustrates a PRBS checker according to an embodiment of the present invention. As shown, PRBS generator 410 is coupled to the input of DUT 420. PRBS checker 430 is coupled to the output of DUT 420. PRBS generator 410 may be the same as PRBS generator 310 of FIG. 3. However, a PRBS generator is not limited to that particular arrangement. Also, DUT 420 may be a communication circuit or channel under test. However, a DUT is not limited to such devices.

PRBS checker 430 includes a shift register chain including R0, R1 and R2. Checker 430 also includes XOR gate RX0, XOR gate RX1, XOR gate RX2, no input sequence detector 432, zero detector 434, one detector 436, error counter 438 and display count 440.

Thus, as illustratively depicted in FIG. 4, the technique uses the same length shift register chain as in FIG. 3 (R0 through R2). Thus, the incoming bits from DUT 420 are shifted directly into the shift register chain which is of the same length as the generator shift register. The outputs of registers R2 and R1 in the receive side are then fed to XOR gate RX0. The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1.

An error in the DUT output stream is immediately flagged as a "1" at the output of RX1. This "1" is delayed by one clock cycle in one detector 436 and is used to invert the output of register R0 using XOR gate RX2. Zero detector 434 is employed to allow enough clock cycles for the generator data to flush (pass) through the DUT and initialize the full shift register length (R0 through R2). Zero detector 434 generates an enable signal after completing its operation to turn on one detector 436.

Error counter 438 counts the errors and display count 440 displays the error count. The error counter may be a conventional binary synchronous counter.

If the number of subsequent zero bits in the output stream of DUT 420 is equal to the length of the shift register chain (R0 through R1), no input sequence detector 432 flags an error. This is done because a PRBS generator cannot generate a sequence of zero bits with a length equal to or greater than the length of shift register chain.

The operation of PRBS checker 430 is further explained by the flow chart of FIG. 5. Although the checker is implemented for a generator with polynomial $X^3 + X^2 + 1$ for simplicity, the inventive techniques can be extended to any PRBS polynomial.

Operation starts at block 502. In step 504, the checker detects "N" zeros at the output of XOR gate RX1. This is done by zero detector 434. It is to be understood that "N" is decided by the designer and equals the number of clock cycles required to flush the DUT plus the number of clock cycles required to flush the checker shift register chain.

In step 506, once "N" zeros are detected, one detector 436 is enabled. In step 508, it is determined whether the output of RX1 equals one. If the output of RX1 equals one, the checker waits one clock cycle (step 510) and then inverts the output of register R0 (step 512). Also, if the output of RX1 equals one, the checker counts the error (step 514) and displays the error count (step 516). The error may be counted by error counter 438 and the error count displayed by count display 440. If the output of RX1 does not equal one (step 508), the step loops until a one is detected.

Further, in step 518, it is determined whether the output of the shift register chain (R0 through R2) is equal to zero. If the output of the shift register chain (R0 through R2) is equal to zero, then no input sequence detector 432 outputs the no PRBS sequence flag (step 520) and the flag is displayed in step 522. If the output of the shift register chain (R0 through R2) does not equal to zero, the step loops until such condition is detected.

Independent claim 6 recites an apparatus for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device. The apparatus comprises a memory, and at least one processor coupled to the memory and operative to: (i) delay the PRBS received by the device to generate a delayed PRBS; (ii) detect the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and (iii) prohibit propagation of the detected error bit in the delayed PRBS; wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

It is to be understood that the apparatus of claim 6 recites similar steps as method claim 1. Therefore, support for the operations performed by the apparatus are described above. Further, page 9, line 8, through page 10, line 5, describe an illustrative processor/memory arrangement for implementing the claimed invention.

Independent claim 11 recites an article of manufacture for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device. The article comprises a machine readable medium containing one or more programs which when executed implement the steps of delaying the PRBS received by the device to generate a delayed PRBS, detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at

least a portion of the PRBS received by the device, and prohibiting propagation of the detected error bit in the delayed PRBS, wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

It is to be understood that the article of claim 11 recites similar steps as method claim 1. Therefore, support for the steps performed by the article are described above. Further, page 9, line 8, through page 10, line 5, describe an illustrative machine readable medium arrangement for implementing the claimed invention.

Independent claim 12 recites apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device. The apparatus comprises a shift register chain, a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS, and at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain.

As described in detail above, FIG. 4 depicts an illustrative embodiment of the claimed invention recited in independent claim 12.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Whether claims 1, 4-6, 9-12 and 17 are anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 4,627,057 to Schmidt et al. (hereinafter "Schmidt").

(2) Whether claims 2 and 7 are unpatentable under 35 U.S.C. §103(a) over Schmidt in view of U.S. Patent No. 5,282,211 to Manlick et al. (hereinafter "Manlick").

(3) Whether claims 3 and 8 are unpatentable under 35 U.S.C. §103(a) over Schmidt in view of U.S. Patent No. 6,215,876 to Gilley (hereinafter "Gilley").

(4) Whether claims 13-16 are unpatentable under 35 U.S.C. §103(a) over Schmidt in view of U.S. Patent Application Publication No. 2002/0063553 to Jungerman (hereinafter "Jungerman").

(5) Whether claims 1, 6 and 11 are unpatentable under 35 U.S.C. §103(a) over Jungerman in view of Schmidt.

ARGUMENT

Appellants incorporate by reference herein the disclosure of their previous responses filed in the present application, namely, the responses dated March 31, 2006 and September 29, 2006.

(1) Whether claims 1, 4-6, 9-12 and 17 are anticipated under 35 U.S.C. §102(b) by U.S. Patent No. 4,627,057 to Schmidt et al. (hereinafter "Schmidt").

Regarding the §102(b) rejection based on Schmidt, Appellants respectfully assert that Schmidt fails to teach or suggest all of the limitations in claims 1, 4-6, 9-12 and 17 for at least the reasons presented below.

It is well-established law that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Appellants assert that the rejection based on Schmidt does not meet this basic legal requirement, as will be explained below.

Independent claim 1 recites a method of checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, the method comprising the steps of: delaying the PRBS received by the device to generate a delayed PRBS; detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and prohibiting propagation of the detected error bit in the delayed PRBS; wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device. Independent claims 6 and 11 recite similar limitations.

Further, original independent claim 12 recites apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device, the apparatus comprising: a shift register chain; a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit

in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS; and at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain.

In Appellants' previous response, it was pointed out that, according to the present specification at page 4, line 14, through page 6, line 9, there are two major types of PRBS checkers. The first type uses a very simple technique as shown in FIG. 2 of the present application. PRBS checker 230 includes a synchronization detector (synchronizing circuit) 232, a local PRBS generator 234 and a comparator circuit 236. Synchronization detector 232 looks for a known pattern in the incoming stream. Once detector 232 detects the known pattern, detector 232 turns on local PRBS generator 234. Local generator 234 and the generator (e.g., 110 in FIG. 1, but not expressly shown in FIG. 2) at the input of DUT 220 are designed to be identical. After synchronization is achieved, the two generators are expected to produce identical bit streams. The comparator circuit 236 detects any mismatches caused due to DUT 220. A major drawback of this technique is the penalty caused due to the synchronizing circuit. These circuits are difficult to build, consume a lot of power as they run at the full rate of incoming data, and their size grows with the length of the generation polynomial.

Appellants respectfully point out that this first approach is the approach taken by Schmidt, i.e., the locally generated signal is the "test signal" described in Schmidt at column 4, lines 29-48.

A second approach uses a self-synchronizing technique as shown in FIG. 3 of the present application. This approach eliminates the need for a synchronizing circuit and local PRBS generation. As explained, PRBS generator 310 includes shift registers T0, T1 and T2, which form a shift register chain. The output of T2 and T1 is fed to an XOR (exclusive OR) gate TX0. The output of TX0 is fed to the input of register T0. Thus, a PRBS of length seven is formed. At any given time, there are three bits in the generator registers (T0 through T2). These three bits identify a single state out of seven states that the generator cycles through. Any new state can be derived from a previous state by the XOR and shift operation. This fundamental principle of generation is

used in the self-synchronizing checker. PRBS checker 330 includes a shift register chain including R0, R1 and R2. Checker 330 also includes XOR gate RX0, XOR gate RX1 and error counter 332. The incoming bits from DUT 320 are shifted directly into the shift register chain which is of the same length as the generator shift register. The outputs of registers R2 and R1 in the receive side are then fed to XOR gate RX0. The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1. Under ideal circumstances, the incoming bit is the same as the RX0 output. Any errors introduced by DUT 320 are then counted by error counter 332.

As further explained in the present application, this second technique has three major drawbacks. First, multiple errors are flagged for a single occurrence. For example, if the DUT sends a bit stream with a single error bit, an error will be flagged at the output of XOR gate RX1 for the first time. This error bit will then propagate from the input of register R0 to the output of R1 after two clock events. When the erroneous bit arrives at the output of R1, the erroneous bit will flag an error for the second time. An error flag will be raised for the third time when this bit reaches the output of R2. Thus, a single error will be flagged three times. A second drawback is that the technique of FIG. 3 masks errors. For example, if in any given incoming stream there are two error bits separated by one, two or three bit positions, these will cancel each other, thus showing no error at all. This is referred to as masking. A third drawback of the technique of FIG. 3 is that if the DUT sends out only zero bits, no error is flagged.

A fundamental reason for flagging of multiple errors and masking is the propagation of an erroneous bit through the shift registers. The present invention realizes that to prevent such an occurrence, the error bit propagation has to be stopped. For example, in a binary system, this error bit can be inverted to its correct value.

The inventions recited in independent claims 1, 6, 11 and 12 address the stated problems with the existing self-synchronizing approach (FIG. 3) by "prohibiting propagation of the detected error bit in the delayed PRBS" (claims 1, 6 and 11), and by "at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain" (claim 12).

Schmidt clearly fails to disclose such a feature since Schmidt is a PRBS checker of the first type, i.e., requiring a local PRBS generator and is not a self-synchronizing PRBS checker.

In the "Response to Amendment" section of the final Office Action, the Examiner states that Schmidt discloses that "the device switches to the safe mode and it transfers the switch process to prohibit propagation of error bit." Further, the Examiner states that "by the fact that error detection in Schmidt . . . will not be instantaneous . . . it is inherent that a delay will be present."

With all due respect, Appellants point out that this rationale seems to ignore the actual limitation of the claim, and ignores the illustrative explanation provided in Appellants' previous response.

The claimed invention recites an explicit step of "delaying the PRBS received by the device to generate a delayed PRBS" and then "comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device to detect the presence of an error bit in the PRBS received by the device ." Right here, Schmidt does not apply because Schmidt does not perform a comparison between the PRBS received by the device and the delayed PRBS. The fact that "error detection in Schmidt . . . will not be instantaneous . . . and it is inherent that a delay will be present," as the Examiner reasons, whether true or not, is irrelevant to the actual language of the claim.

Further, the claimed invention recites an explicit step of "prohibiting propagation of the detected error bit in the delayed PRBS." It is understood that the claim is explicitly stating that the propagation of the detected error bit in the delayed PRBS is being prohibited. Illustrative examples of how this is done are mentioned above and described in the present specification, e.g., in a binary system, the error bit is inverted to its correct value thus prohibiting propagation of the error bit. The fact that Schmidt switches to some kind of safe mode, is not the same as prohibiting propagation of the detected error bit in the delayed PRBS, as the claimed invention recites.

For at least the above reasons, Appellants assert that claims 1, 4-6, 9-12 and 17 are patentable over Schmidt.

Appellants further assert that dependent claims 4, 5, 9, 10 and 17 recite patentable subject matter in their own right.

By way of example, claims 4, 9 and 17 recite detecting the non-presence of a PRBS from the device. The final Office Action cites Schmidt at column 6, lines 4-10. However, such portion of Schmidt mentions nothing about an actual, express step of detecting the non-presence of a PRBS from the device. Schmidt refers to an "impermissible condition 00000000." However, this condition is not detected, nor is it necessarily representative of the non-presence of a PRBS.

(2) Whether claims 2 and 7 are unpatentable under 35 U.S.C. §103(a) over Schmidt in view of U.S. Patent No. 5,282,211 to Manlick et al. (hereinafter "Manlick").

Appellants assert that claims 2 and 7 are patentable over the Schmidt/Manlick combination for at least the reasons given above with respect to claims 1 and 6. Manlick fails to remedy the deficiencies of Schmidt.

Appellants further assert that dependent claims 2 and 7 recite patentable subject matter in their own right.

Claims 2 and 7 recite that the prohibition step/operation serves to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the PRBS received by the device. The final Office Action at page 8 states that "Schmidt et al. does not explicitly teach the incorporation of a counter during testing." Then, the final Office Action cites a counter being disclosed in Manlick. However, even if properly combinable, Appellants do not see how these two references teach or suggest the claim limitations that a prohibition step/operation serves to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the PRBS received by the device. First, there is no prohibition step/operation disclosed by the combination. Secondly, neither reference even mentions a need to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the PRBS received by the device.

Further, Appellants assert that the Examiner has failed to provide legally sufficient rationale for combining the two references.

(3) Whether claims 3 and 8 are unpatentable under 35 U.S.C. §103(a) over Schmidt in view of U.S. Patent No. 6,215,876 to Gilley (hereinafter "Gilley").

Appellants assert that claims 3 and 8 are patentable over the Schmidt/Gilley combination for at least the reasons given above with respect to claims 1 and 6. Gilley fails to remedy the deficiencies of Schmidt.

Appellants further assert that dependent claims 3 and 8 recite patentable subject matter in their own right.

Claims 3 and 8 recite that the prohibition step further comprises correcting the error bit. The final Office Action at page 10 states that "Schmidt et al. does not explicitly teach the correction of the error bit." Then, the final Office Action cites a error correction being disclosed in Gilley. However, even if properly combinable, Appellants do not see how these two references teach or suggest the claim limitations that a prohibition step/operation comprises correcting the error bit. There is no prohibition step/operation disclosed by the combination.

Further, Appellants assert that the Examiner has failed to provide legally sufficient rationale for combining the two references.

(4) Whether claims 13-16 are unpatentable under 35 U.S.C. §103(a) over Schmidt in view of U.S. Patent Application Publication No. 2002/0063553 to Jungerman (hereinafter "Jungerman").

Appellants assert that claims 13-16 are patentable over the Schmidt/Jungerman combination for at least the reasons given above with respect to claim 12. Jungerman fails to remedy the deficiencies of Schmidt.

Appellants further assert that dependent claims 13-16 recite patentable subject matter in their own right.

Claim 13 recites a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and initialize the full length of the shift register chain. Claim 14 recites wherein the second logic detector generates an enable signal after completing its operation so as to turn on the at least one logic detector. Claim 15 recites an error counter coupled to the logic gate for counting errors detected between the input

PRBS and the output PRBS. Claim 16 recites an error count display coupled to the error counter for displaying the error count.

While the Examiner admits that Schmidt fails to disclose such claim limitations, the final Office Action attempts to combine Schmidt with a non-analogous reference that discloses a system for displaying a waveform on an error performance analyzer (Jungerman). Even if Jungerman were to show an error counter or error count display, it has nothing to do with checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device.

Thus, Appellants assert that the Examiner has failed to provide legally sufficient rationale for combining the two references.

(5) Whether claims 1, 6 and 11 are unpatentable under 35 U.S.C. §103(a) over Jungerman in view of Schmidt.

The Examiner also rejects claims 1, 6 and 11 based on a combination of Jungerman and Schmidt. However, the same deficiencies pointed out above with respect to Schmidt alone are present in the combination.

In fact, the final Office Action at page 15 admits that Jungerman fails to disclose the step of prohibiting propagation of the detected error bit in the delayed PRBS. However, the Examiner relies on Schmidt for this claim limitation. However, as explained above, Schmidt does not provide such an actual, express step/operation.

Further, Appellants assert that the Examiner has failed to provide legally sufficient rationale for combining the two references.

In view of the above, Applicants believe that claims 1-17 are in condition for allowance, and respectfully request withdrawal of the various §102(b) and §103(a) rejections.

Respectfully submitted,

Date: December 4, 2006

William E. Lewis
Attorney for Applicant(s)
Reg. No. 39,274
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-2946

APPENDIX

1. A method of checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, the method comprising the steps of:

delaying the PRBS received by the device to generate a delayed PRBS;

detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and

prohibiting propagation of the detected error bit in the delayed PRBS;

wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

2. The method of claim 1, wherein the prohibition step serves to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the PRBS received by the device.

3. The method of claim 1, wherein the prohibition step further comprises correcting the error bit.

4. The method of claim 1, further comprising the step of detecting the non-presence of a PRBS from the device.

5. The method of claim 1, wherein the device is one of a communication circuit and a communication channel.

6. Apparatus for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, the apparatus comprising:

a memory; and

at least one processor coupled to the memory and operative to: (I) delay the PRBS received by the device to generate a delayed PRBS; (ii) detect the presence of an error bit in the PRBS

received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and (iii) prohibit propagation of the detected error bit in the delayed PRBS; wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

7. The apparatus of claim 6, wherein the prohibition operation serves to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the PRBS received by the device.

8. The apparatus of claim 6, wherein the prohibition operation further comprises correcting the error bit.

9. The apparatus of claim 6, wherein the processor is further operative to detect the non-presence of a PRBS from the device.

10. The apparatus of claim 6, wherein the device is one of a communication circuit and a communication channel.

11. An article of manufacture for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, comprising a machine readable medium containing one or more programs which when executed implement the steps of:

delaying the PRBS received by the device to generate a delayed PRBS;

detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and

prohibiting propagation of the detected error bit in the delayed PRBS;

wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

12. Apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device, the apparatus comprising:

a shift register chain;

a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS; and

at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain.

13. The apparatus of claim 12, further comprising a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and initialize the full length of the shift register chain.

14. The apparatus of claim 13, wherein the second logic detector generates an enable signal after completing its operation so as to turn on the at least one logic detector.

15. The apparatus of claim 12, further comprising an error counter coupled to the logic gate for counting errors detected between the input PRBS and the output PRBS.

16. The apparatus of claim 15, further comprising an error count display coupled to the error counter for displaying the error count.

17. The apparatus of claim 12, further comprising a third logic detector coupled to the shift register chain for detecting the non-presence of a PRBS from the device.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.